MUSIC™ SEMICONDUCTORS

TR9C1710
GRAPHICS COLOR PALETTE

PRELIMINARY SPECIFICATION

DISTINCTIVE CHARACTERISTICS

- **Combination Look-up Table and Triple Video DAC**
- **Directly drives single- and double-terminated 75-ohm transmission lines**
- **Displays 256 colors from a palette of 256K colors**
- **Asynchronous Microprocessor interface**
- **Read and Write contents of Look-up Table**
- **VGA, Super VGA, VESA, TIGA™, and 8514/A compatible with enhanced features**
- **Unlimited access to Look-up Table; no need to wait for retrace**
- **Unlimited access to Mask Register**
- **28-pin PDIP and 32- and 44-pin PLDCC Packages**
- **Available in 80-, 66-, 50-, and 35-MHz Pixel Rates**
- **High-Performance CMOS for low operating power**
- **TTL-compatible inputs**

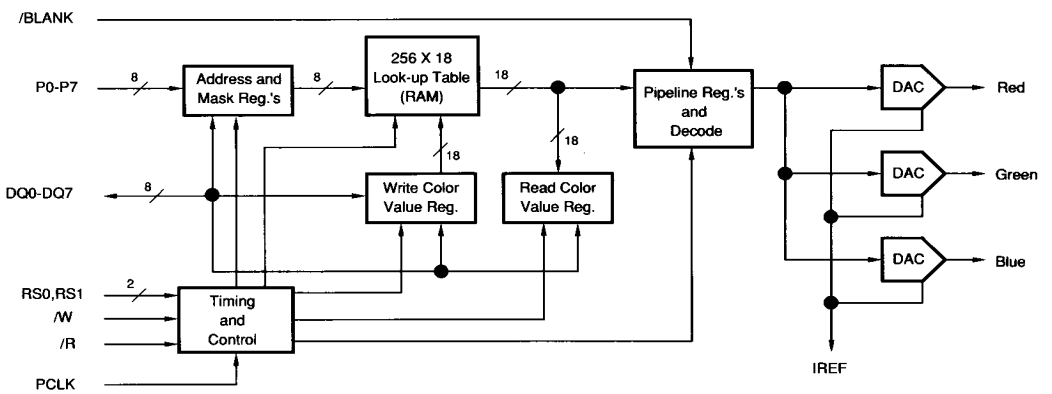
GENERAL DESCRIPTION

The TR9C1710 is a monolithic 256-word by 18-bit Look-up Table and Triple Video DAC, with 6-bit DACs. The Look-up Table accepts up to eight bits per pixel from the Frame Buffer and performs a translation into three 6-bit values for conversion into Red, Green, and Blue analog signals. Each of the Video DACs can directly drive a double-terminated 75-ohm transmission line.

The TR9C1710 incorporates a proprietary feature called Pixel Replicate™ that allows both Read and Write operations to occur to the Look-up Table when the display is active without causing random noise on the screen.

The TR9C1710 is available in standard 28-pin DIP and 32- and 44-pin PLDCC packages and supports the screen resolutions and color capacity necessary for high-performance Personal Desktop Computers and Workstation Graphics systems. The TR9C1710 is fully compatible with VGA and Super-VGA industry standards.

BLOCK DIAGRAM



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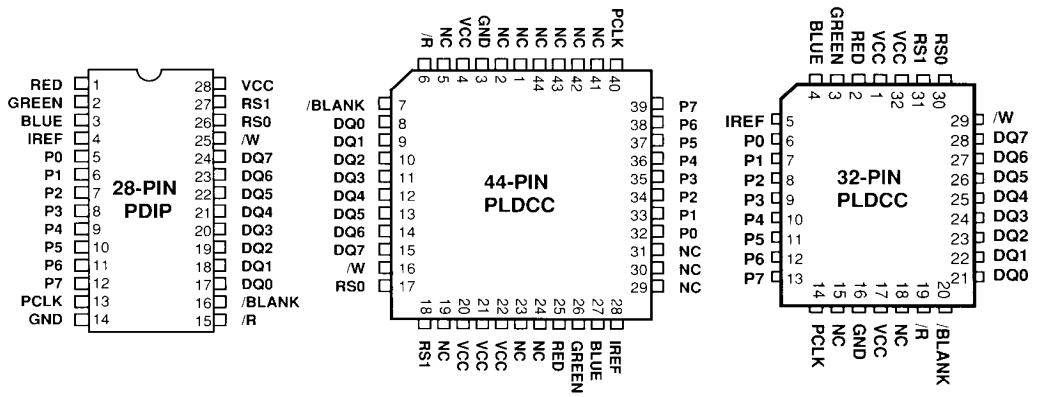
September 15, 1991, Rev. 1

TR9C1710

PINOUT DIAGRAMS



PIN DESCRIPTION

Red, Green, Blue (Analog Outputs) (Note 10)

These signals are the outputs of the three video DAC's which drive doubly or singly terminated 75-ohm transmission lines and can directly drive a suitable monitor or video amplifier.

IREF (Current Reference)

IREF provides a current reference for the TR9C1710's Video DACs. IREF must be driven by an external current sink providing a regulated current. Each current source in the DAC will contribute IREF/30 current to the output. The value for IREF is given by the equation:

$$IREF = \frac{30 \times V_{WHITE}}{63 \times R_{LOAD}}$$

P0-P7 (Pixel Address 0-7, TTL Input)

P0-P7 are registered on the rising edge of PCLK and are the addresses used to reference a color value stored in the Look-up Table for conversion to analog video signals. Individual Pixel Address bits are ANDed with the corresponding Mask Register bits.

PCLK (Pixel Clock, TTL Input, Rising Edge Active)

The Pixel Clock registers the Pixel Address (P0-P7), transfers data in the internal pipeline, and synchronizes the Microprocessor Port signals. Each Pixel Clock period corresponds to one pixel displayed on the monitor.

/BLANK (Blank Control, TTL Input, Active LOW)

The state of the /BLANK input is registered by the rising edge of PCLK. The /BLANK signal is used for blanking the display during retrace. With /BLANK HIGH, the DAC outputs reflect their digital input values. When /BLANK is LOW, the DAC outputs are forced to the Blanking Level. /BLANK has the same pipeline delay as P0-P7.

/R (Read, TTL Input, Active LOW)

The Falling edge of /R registers the states of RS0-RS1, which are decoded to determine the source of the read data. The outputs become valid after the access time elapses from the falling edge of /R and high-impedance after the rising edge of /R.

/W (Write, TTL Input, Active LOW)

The Falling edge of /W registers the states of RS0-RS1, which are decoded to determine the destination for the write data. The input data must meet set-up and hold times referenced to the rising edge of the /W signal.

DQ0-DQ7 (Data Bus, I/O, Three-state TTL)

All Data transfers to and from the Microprocessor Port occur over DQ0-DQ7. The Mask Register and the Read/Write Address Register use all 8 bits, while Color Values use only the lower order six bits (DQ0-DQ5).

RS0, RS1 (Register Select 0-1, TTL Inputs)

The Register to be read or written during a Microprocessor Port cycle is determined by the state of RS0 - RS1 at the beginning of the cycle. The beginning of the cycle is initiated by the falling edge of either /R or /W, depending on the type of cycle. The chart below indicates the Register Assignments as a function of RS0 and RS1.

RS1	RS0	Register Assignment
0	0	Pixel Address Register (RAM Write)
0	1	Color Value
1	0	Pixel Mask Register
1	1	Pixel Address Register (RAM Read)

FUNCTIONAL DESCRIPTION

OVERVIEW

The TR9C1710 consists of a 256-word by 18-bit Look-up Table, a Mask register which is ANDed with the Look-up Table's address, a Triple six-bit Video DAC, along with the logic needed to implement a Microprocessor interface for accessing the Mask register and the Look-up table.

The TR9C1710 has three distinct sections. The first section consists of the Pixel address (P0-P7), /BLANK, and Pixel Clock (PCLK). The states of P0-P7 and /BLANK are captured at the rising edge of PCLK, corresponding to each pixel. The second section contains the 256x18 Look-up table (RAM) and the Video DACs used to drive an analog monitor. The third section contains the microprocessor port, which is used to access the Look-up table and Mask register.

VIDEO INPUT

P0-P7 are ANDed with the contents of the Mask register and passed as an address to the Look-up table. The Mask register is fully synchronized. If the Mask register contains the byte value FFH, then the state of the P0-P7 is unaltered. If the Mask register contains 00H, then the Look-up table will be passed 00H. The contents of the location pointed to by the eight-bit address passed to the Look-up table is accessed with the 18-bit result transferred to the Video DACs.

The /BLANK (active LOW) input is used to blank the display during retrace. A LOW level on /BLANK will force the Video DACs to the Blanking Level without reference to the output of the Look-up table. A HIGH level on /BLANK will allow the output of the Look-up table to be converted into analog levels by the DACs. The pipeline delay for /BLANK is identical to the delay of the P0-P7 path through the Look-up table.

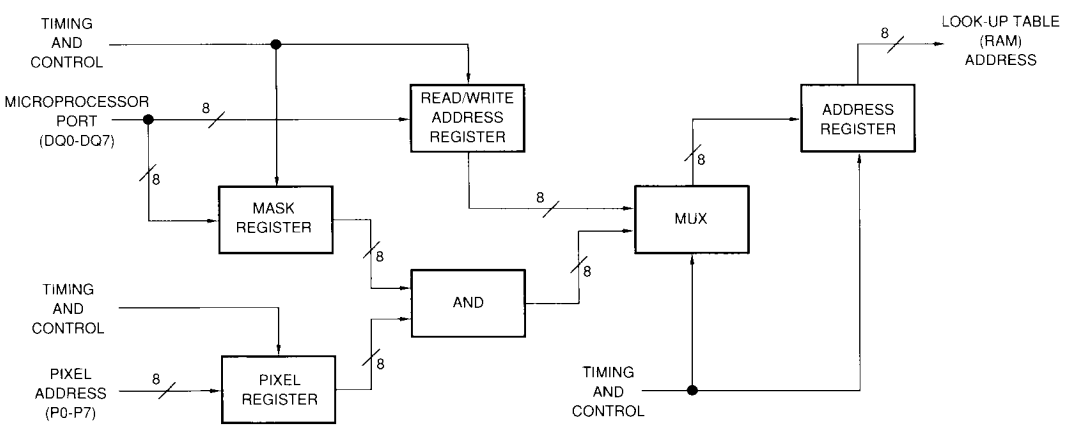
MICROPROCESSOR INTERFACE

The Microprocessor interface is used to access the Look-up table's RAM array (256 words of 18 bits). The TR9C1710 is designed to allow operations on the Look-up table at any time without waiting for retrace. Microprocessor Interface operations and Video Input cycles are synchronized with PCLK such that one Video cycle is borrowed for each 18-bit Microprocessor-interface-to-Look-up-table transfer (read or write). While this cycle is being borrowed, the data from the previous Pixel value is replicated at the DAC outputs. This feature, called Pixel Replicate™, eliminates the snow on the screen that can result from borrowing a Video cycle during active display time.

The eight-bit Mask register is programmed by the Host Processor by a Write cycle with RS0 = 0 and RS1 =1. The states of RS0 and RS1 are captured on the falling edge of /W and the state of the data bus (DQ0-DQ7) is captured on the rising edge of /W. The Mask register may be read by performing a Read cycle, again with RS0 = 0 and RS1 =1. The states of RS0 and RS1 are captured on the falling edge of /R, with the contents of the Mask register placed on the Data bus (DQ0-DQ7). The Data bus will remain active until after the rising edge of /R after which it will assume a high-impedance state.

The Look-up table is accessed by using the three registers: the Read/Write Address register (eight bits), the Color Value Write register (18 bits), or Color Value Read register (18 bits). Before any data can be placed into the Look-up table, the contents of the Read/Write Address register must be initialized by a Write cycle with RS0 = 0 and RS1 = 0. The address is then placed on the Data bus. After the Read/Write Address register is initialized, the Color Value Write register

ADDRESS LOGIC



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FUNCTIONAL DESCRIPTION (CONT'D)

is programmed with the information that is to be written into the selected address. This operation comprises three Write cycles to the Color Value Write register with RS0=1 and RS1=0 and with the data on DQ0-DQ5. The first Write cycle is the Red field, followed by the Green and the Blue. After the third Write cycle (Blue), the contents of the Color Value Write register are written into the memory at the address in the Read/Write Address register, and the Read/Write Address register is incremented, allowing sequential addresses to be written without the need to rewrite the Read/Write Address register.

The contents of the Look-up table may be read by performing a Write cycle to the Read/Write Address register (RS0 =1 and RS1=1). The contents of the addressed location in the Look-up table are then accessed and placed in the Color Value Read register and the Address register is incremented. The contents of the Color Value Read register are then read by performing Read cycles with RS0=1 and RS1=0. The first Read cycle returns the Red field, followed by the Green and then the Blue on subsequent Read cycles. The data is output on DQ0-DQ5. After the third Read cycle (Blue Data), the address stored in the Read/Write Address register (already incremented) is accessed with its contents placed in the Color Value Read register. Sequential addresses may then be read without reprogramming the Read/Write Address register.

TRIPLE VIDEO DAC

The Triple Video DAC consists of three six-bit DACs capable of directly driving a doubly terminated 75-ohm transmission line (75-ohm termination resistors to ground at both ends of the line). Each DAC consists of 63 identical current sources, which are selected through a six-bit binary decoder resulting in 64 levels per DAC. With /BLANK LOW, the DAC output is the same as the Black level (all current sources off). The pipeline delay for P0-P7 is the same (four registers in the pipeline, three clock delays) as the delay for /BLANK.

The DACs may also be used to drive analog monochrome displays. One of the DAC outputs can be connected to the single video input of a monochrome monitor (see Note 10). If the video frame buffer contains information intended for display on a color monitor, the Look-up table can be reprogrammed to provide only the intensity portion of the color information. This technique allows the display of a digitized color frame in monochrome.

APPLICATIONS

The TR9C1710 incorporates two common graphics functions: a Look-up table and D/A Converters (in the form of a Triple Video DAC). The TR9C1710 provides a wide range of capabilities for a color or monochrome system. The TR9C1710 can display up to 256 colors at a time, each of which can be any combination of the 64 levels available from each of the three DACs. The TR9C1710 can display pseudo-color images where the various shades of a monochrome image are assigned unique colors, allowing image processing techniques, such as density slicing, to be easily implemented on monochrome digitized images. Density slicing is a technique for viewing monochrome images in color by assigning each gray-scale level a unique color for display. Small differences in intensity (one bit of the gray-scale) are difficult for the eye to differentiate in monochrome, but become readily apparent when assigned unique colors. Changing only the contents of the Look-up table can transform the displayed image from monochrome into color.

SYSTEM DESIGN CRITERIA

VCC and ground planes are recommended for the TR9C1710 power distribution system. A 0.01uF and a 100pF high-frequency decoupling capacitors should be placed between the VCC and ground planes as near to the device as possible.

The signal lines connected to the /BLANK, P0-P7 and PCLK inputs must be either very short or terminated. It is recommended that a register be used adjacent to the TR9C1710's package to ease the timing constraints and eliminate any possibility of ringing or undershoot. This device is fabricated in CMOS technology, with high-impedance inputs that do not clamp to ground. If the P0-P7 signals are to be multiplexed, the use of three-state outputs is not recommended. Unprotected CMOS inputs should never be directly connected to traces that run off the PCB.

The IREF terminal requires a well-regulated current sink for proper operation (current flows to ground). Many different approaches to the design of the regulated current sink may be used, as long as the voltage on the IREF pin does not go below ground. Neither a resistor to a negative supply voltage nor a variable resistor is recommended. The IREF terminal may be isolated from noise by using a series inductance between IREF and the external current sink. Better results are obtained when IREF is not capacitively coupled to VCC.

This information is intended solely to stimulate design ideas. MUSIC™ accepts no liability for conceptual designs suggested herein. All users are cautioned to verify their own designs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 Volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns, measured at the 50% point)
Temperature Under Bias	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Maximum Reference Current	-15 mA
Maximum DAC Output Current	45 mA (per Output)
Maximum DC TTL Output Current	20 mA (per Output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to GND at the device pins.

OPERATING CONDITIONS

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts	
V_{IH1}	Input Voltage Logic "1" (all inputs except /W, /R)	2.0		VCC+0.5	Volts	
V_{IH2}	Input Voltage Logic "1" (/W, /R only)	2.2		VCC+0.5	Volts	
V_{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	-1.0 Volts for 10 ns measured 50% amplitude (Fig. 4)
T_A	Ambient Operating Temperature	0		70	°C	Still Air
I_{REF}	Reference Current	-3.5	-8.88	-10	mA	

ELECTRICAL CHARACTERISTICS (TTL-COMPATIBLE SIGNALS)

Symbol	Parameter	Min	Max	Units	Note
I_{CC}	Average Power Supply Current		110	mA	PCLK=35 MHz; 1
			120	mA	PCLK = 50, 66 MHz; 1
			130	mA	PCLK = 80 MHz; 1
V_{OH}	Output Voltage Logic "1"	2.4		Volts	I_{OH} = -5.0 mA
V_{OL}	Output Voltage Logic "0"		0.4	Volts	I_{OL} = 5.0 mA
I_{ILK}	Input Leakage Current	-2	2	µA	$V_{GND} \le V_{IN} \le V_{CC}$
I_{OLK}	Leakage Current (DQ0-DQ7)	-10	10	µA	$V_{GND} \le V_{IN} \le V_{CC}$, /R ≥ V_{IH} (min)

DAC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Notes
V_{REF}	Voltage on I_{REF}	V_{CC} -3.0	V_{CC}	Volts	-10.0 ≤ I_{REF} ≤ -3.5 mA
V_O MAX	Maximum Output Voltage		1.5	Volts	$I_O \le$ 10 mA; 10
I_O MAX	Maximum Output Current	21		mA	$V_O \le$ 1.0 Volts
	Resolution	6		bits	
	Full Scale Error		± 6	%	2
	DAC to DAC Correlation		0.5	%	3
	Integral Nonlinearity		±0.5	LSB	4
	Rise Time (DAC Output)		6	ns	6; 10 to 90%; Load shown in Figure 1
	Full Scale Settling Time		12.5	ns	5, 6; Load shown in Figure 1
	Glitch Energy		40	pV-sec	6; Load shown in Figure 1

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SWITCHING TEST CIRCUITS

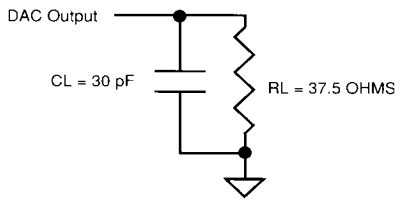


Figure 1

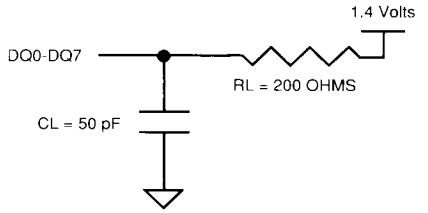


Figure 2

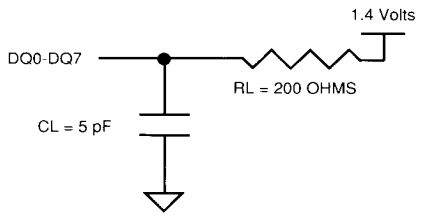


Figure 3

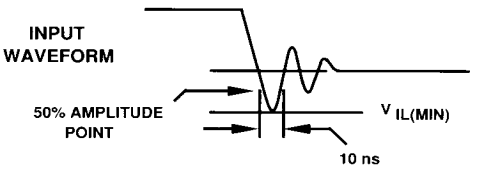


Figure 4

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 Volts
Input Signal Rise and Fall Times	≤ 3 ns
Digital Input Timing Reference Level	1.5 Volts
Digital Output Timing Reference Levels	.8V and 2.4V
DAC Switching Test Load	Figure 1
TTL Switching Test Load	Figure 2

CAPACITANCE

T_A = 0 to 70°C; V_{CC} = 5.0V± 10%; f = 1.0 MHz

Symbol	Parameter	Max	Notes
CI	Digital Input	7 pF	6, Pins 5 - 13 , 15 - 16 , 25 - 27
CO	Digital Output	7 pF	6, Pins 17 - 24
COA	Analog Output	10 pF	6, 9; Pins 1 - 3

SWITCHING CHARACTERISTICS

VIDEO PORT

			TR9C1710-80		TR9C1710-66		TR9C1710-50		TR9C1710-35			
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	t_{CHCH}	PCLK Period	12.5		15		20		28		ns	
2	t_{CLCH}	PCLK LOW	4		5		6		9		ns	
3	t_{CHCL}	PCLK HIGH	4		5		6		7		ns	
4	t_{PVCH}	Pixel setup	3		3		3		4		ns	
5	t_{CHPX}	Pixel hold	3		3		3		4		ns	
6	t_{BVCH}	BLANK setup	3		3		3		4		ns	
7	t_{CHBX}	BLANK hold	3		3		3		4		ns	
8	t_{CHAV}	PCLK to DAC valid	0	20	0	20	0	25	0	3	ns	7
8a	t_{CHAV} (skew)	DAC to DAC Skew		1		1		1		1	ns	7

MICROPROCESSOR PORT READ CYCLE

			All Speed Grades				
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Units**	**Notes**	
9	t_{RLRH}	Read Pulse Width	50		ns		
10	t_{RHRL1}	Successive Read Interval	3 X t_{CHCH}		ns		
11	t_{RHWL1}	Read to Write	3 X t_{CHCH}		ns		
12	t_{RHRL2}	Color Read to Read	6 X t_{CHCH}		ns		
13	t_{RHWL2}	Color Read to Write	6 X t_{CHCH}		ns		
14	t_{SVRL}	Register Select Setup	10		ns		
15	t_{RLSX}	Register Select Hold	3		ns		
16	t_{RLQV}	Data Access from /R		40	ns		
17	t_{RLQX}	Output turn-on from /R	3		ns		
18	t_{RHQX}	Data hold from /R	3		ns		
19	t_{RHQZ}	Data Three-state Delay		20	ns	8	

SWITCHING CHARACTERISTICS (CONT'D)

MICROPROCESSOR PORT WRITE CYCLE

			All Speed Grades				
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Units**	**Notes**	
20	t_{WLWH}	Write Pulse Width	50		ns		
21	t_{WHW1}	Successive Write Interval	3 X t_{CHCH}		ns		
22	t_{WHW2}	Write After Color Write	3 X t_{CHCH}		ns		
23	t_{WHRL1}	Write to Read	3 X t_{CHCH}		ns		
24	t_{WHRL2}	Color Write to Read	3 X t_{CHCH}		ns		
25	t_{WHRL3}	Read after Read Address Write	6 X t_{CHCH}		ns		
26	t_{SVWL}	Register Select setup	10		ns		
27	t_{WLSX}	Register Select hold	3		ns		
28	t_{DVWH}	Data setup to /W HIGH	10		ns		
29	t_{WHDX}	Data hold from /W HIGH	3		ns		

NOTES

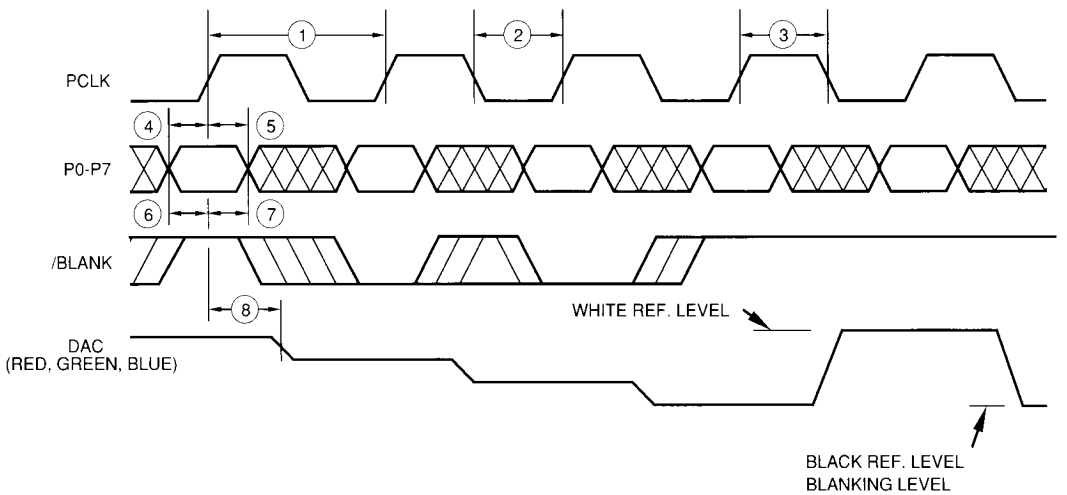
1. ICC is measured with VCC = VCC (max) and tCHCH = tCHCH (min). The DAC test load is as shown in Figure 1. DQ0-DQ7 are unloaded. IREF = -8.88 mA.
2. Full Scale Error is measured from the value given by the design equation. IREF = -8.88 mA.
3. Measured from the DAC output with the center value. IREF = -8.88 mA.
4. Measured from a straight line between the endpoints. Monotonicity is guaranteed.
5. Full Scale Settling Time is measured from a 2% change in output voltage until the output voltage has settled to within ± 2% of final value.
6. Guaranteed but not 100% tested.
7. Measured at the 50% point between the starting and ending DAC values.
8. Measured from a ± 200 mV change from the steady-state voltage using Test Load as shown in Figure 3.
9. /BLANK ≤ VIL (MAX) to Disable RED, GREEN, and BLUE Analog outputs.
10. All DAC outputs must be terminated and not left floating. The equivalent of a double- or single-terminated 75-ohm transmission line (37.5-ohm or 75-ohm resistive load), can be used. Unused DAC outputs may also be directly tied to ground.

SWITCHING WAVEFORM

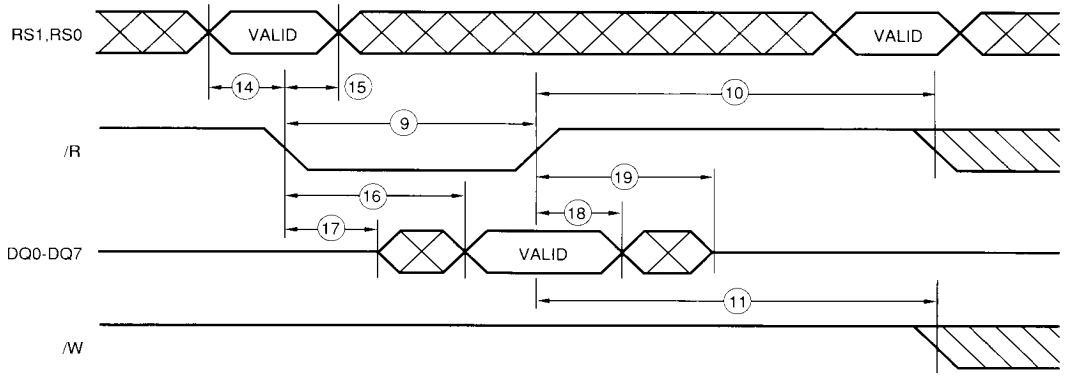
KEY

WAVEFORMS	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care. Any change permitted	Undefined. State unknown
	Does not apply	Center line is high impedance "off state"

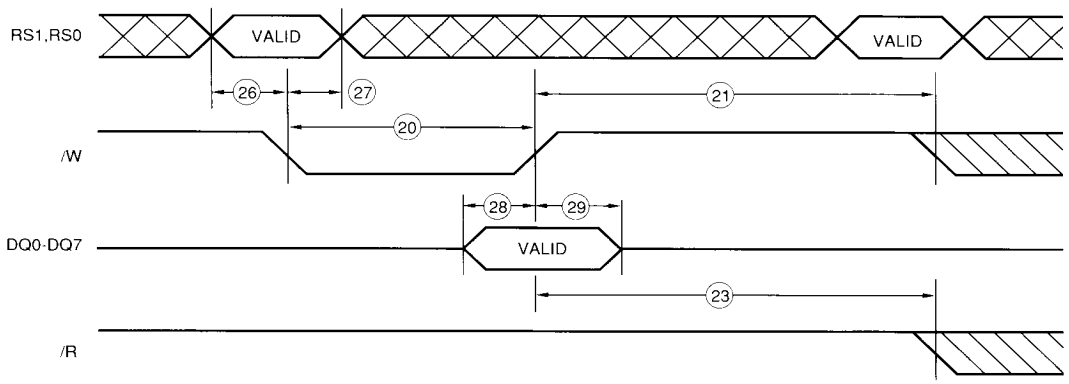
VIDEO TIMING



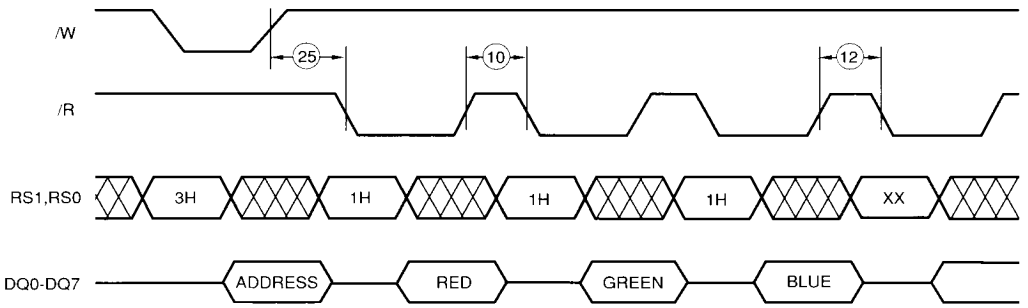
MICROPROCESSOR READ CYCLE



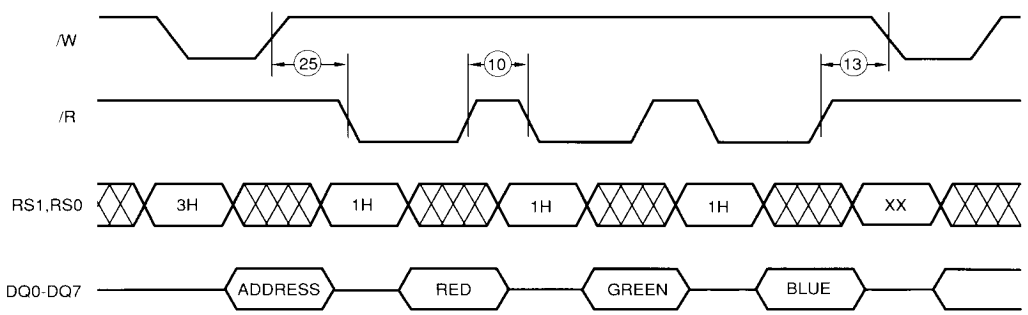
MICROPROCESSOR WRITE CYCLE



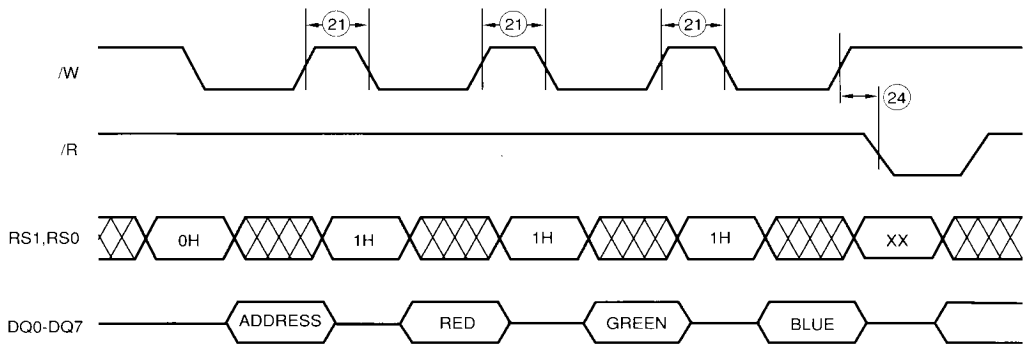
COLOR VALUE READ TO READ



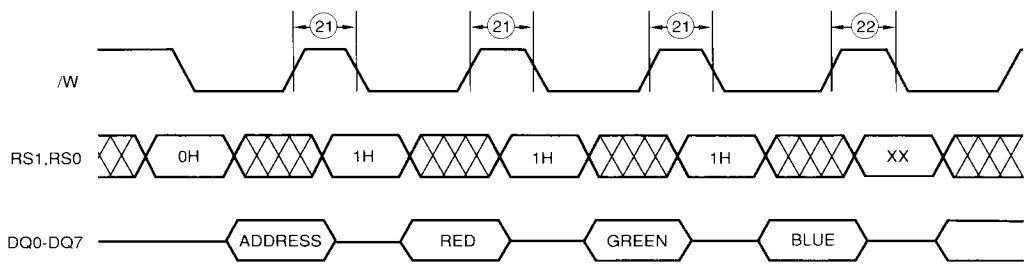
COLOR VALUE READ TO WRITE



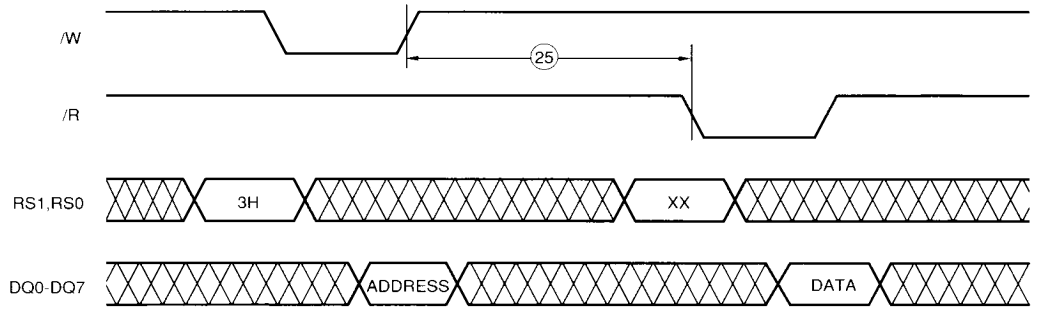
READ AFTER COLOR VALUE WRITE



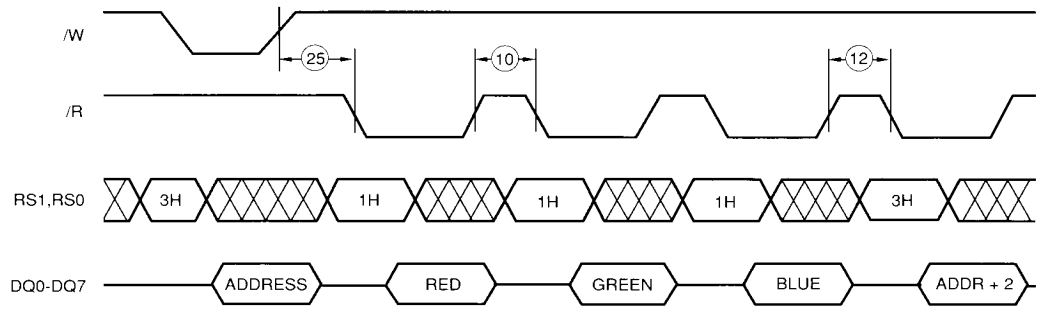
WRITE AFTER COLOR VALUE WRITE



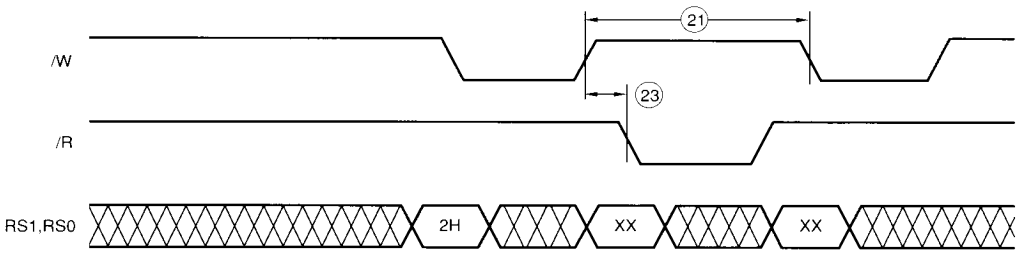
READ AFTER WRITING READ ADDRESS REGISTER



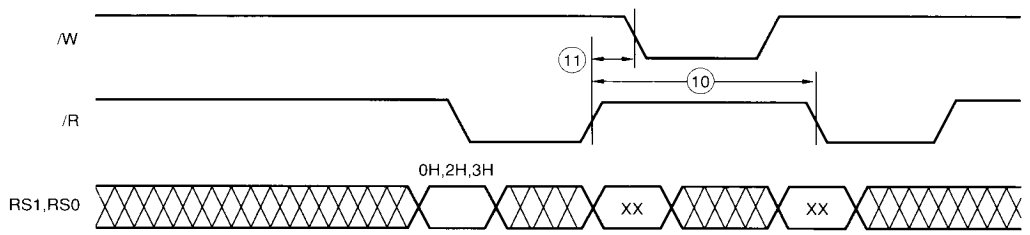
READ COLOR VALUE THEN READ ADDRESS



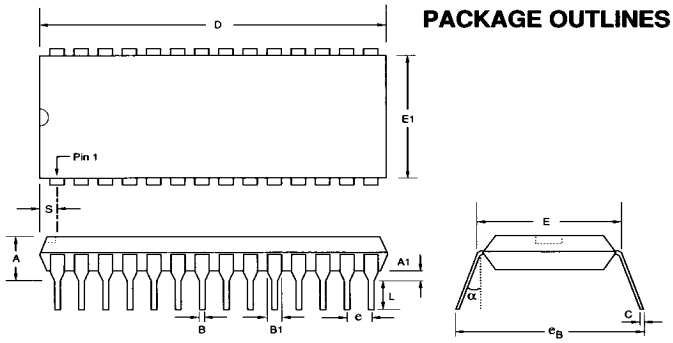
MASK REGISTER WRITE TO READ OR WRITE



READ FROM MASK OR ADDRESS REGISTER TO READ OR WRITE

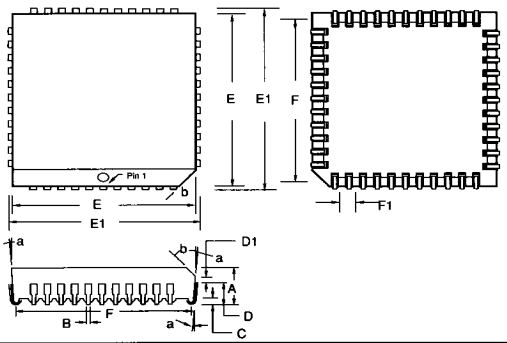


PACKAGE OUTLINES



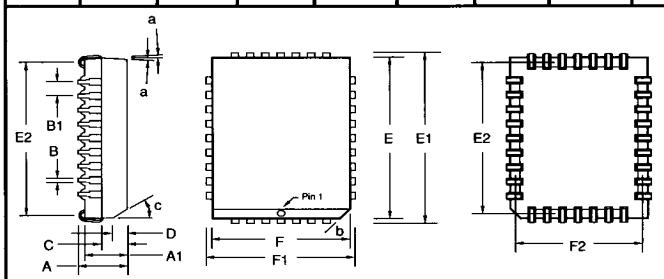
28-PIN PLASTIC 600-MIL DIP

Lead Count	Dim. A	Dim. A1	Dim. B	Dim. B1	Dim. C	Dim. D	Dim. E	Dim. E1	Dim. e	Dim. e_B	Dim. L	Dim. S	Dim. α
28	.170 .210	.020 .050	.015 .020	.055 .065	.008 .013	1.440 1.460	.590 .610	.540 .560	.090 .110	.640 .690	.125 min	.025 .070	0° 15°



44-PIN PLASTIC LEADED CHIP CARRIER

Lead Count	Dim A	Dim B	Dim C	Dim D	Dim D1	Dim E	Dim. E1	Dim. F	Dim. F1	Dim. a	Dim. b		
44	.170 .176	.017 TYP	.033 .043	.098 TYP	.050 TYP	.650 .656	.685 .695	.620 .626	.050 TYP	3^0 6^0	45^0 TYP		



32-PIN PLASTIC LEADED CHIP CARRIER

Lead Count	Dim A	Dim A1	Dim B	Dim B1	Dim C	Dim D	Dim E	Dim E1	Dim E2	Dim F	Dim F1	Dim F2	Dim a	Dim b	Dim c
32	.131 .141	.110 TYP	.017 TYP	.050 TYP	.041 TYP	.025 TYP	.547 .553	.584 .596	.505 .525	.447 .453	.485 .495	.405 .425	3° 6°	45° TYP	30° TYP

All dimensions are in inches and degrees and are min/max except where noted.

Rev.1

TR9C1710

ORDERING INFORMATION

Part Number	Speed	Package	Temperature Range
TR9C1710-**XXY**C			0 to 70°C
XX= 35	35 MHz		
XX= 50	50 MHz		
XX= 66	66 MHz		
XX= 80	80 MHz		
Y= P		28-pin, Plastic DIP	
Y= D		44-pin, PLDCC	
Y= E		32-pin, PLDCC	

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